**UNIT – II OPERATIONAL AMPLIFIER**

**Objective**

The purpose of these experiments is to introduce the most important of all analog

building blocks, the *operational amplifier* (“op-amp” for short). This handout gives an introduction to these amplifiers and a smattering of the various configurations that they can be used in. Apart from their most common use as amplifiers (both inverting and non-inverting), they also find applications as buffers (load isolators), adders, subtractors, integrators, logarithmic amplifiers, impedance converters, filters (low-pass, high-pass, band-pass, band-reject or notch), and differential amplifiers. So let’s get set for a fun-filled adventure with op-amps!

**General Operational Amplifier:**

An operational amplifier generally consists of three stages, anmely,1. a differential

amplifier 2. additional amplifier stages to provide the required voltage gain and dc level shifting 3. an emitter-follower or source follower output stage to provide current gain and low output resistance. A low-frequency or dc gain of approximately 104 is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp. The output voltage is required to be at ground, when the differential input voltages is zero, and this necessitates the use of dual polarity supply voltage. Since the output resistance of op-amp is required to be low, a complementary push-pull emitter – follower or source follower output stage is employed. Moreover, as the input bias currents are to be very small of the order of picoamperes, an FET input stage is normally preferred. The figure shows a general op-amp circuit using JFET input devices.

**Input stage:**

The input differential amplifier stage uses p-channel JFETs M1 and M2. It employs a three transistor active load formed by Q3 , Q4 , and Q5 . the bias current for the stage is provided by a two-transistor current source using PNP transistors Q6 and Q7. Resistor R1 increases the output resistance seen looking into the collector of Q4 as indicated by R04. This is necessary to provide bias current stability against the transistor parameter variations. Resistor R2 establishes a definite bias current through Q5 . A single ended output is taken out at the collector of Q4 . MOSFET‘s are used in place of JFETs with additional devices in the circuit to prevent any damage for the gate oxide due to electrostatic discharges.

**Gain stage:**

The second stage or the gain stage uses Darlington transistor pair formed by Q8 and Q9 as shown in figure. The transistor Q8 is connected as an emitter follower, providing large input resistance. Therefore, it minimizes the loading effect on the input differential amplifier stage. The transistor Q9 provides an additional gain and Q10 acts as an active load for this stage. The current mirror formed by Q7 and Q10 establishes the bias current for Q9 . The VBE drop across Q9 and drop across R5 constitute the voltage drop across R4 , and this voltage sets the current through Q8 . It can be set to a small value, such that the base current of Q8 also is very less.

**Output stage:**

The final stage of the op-amp is a class AB complementary push-pull output stage. Q11 is an emitter follower, providing a large input resistance for minimizing the loading effects on the gain stage. Bias current for Q11 is provided by the current mirror formed by Q7 and Q12, through Q13 and Q14 for minimizing the cross over distortion. Transistors can also be used in place of the two diodes. The overall voltage gain AV of the op-amp is the product of voltage gain of each stage as given by AV = |Ad | |A2||A3| Where Ad is the gain of the differential amplifier stage, A2 is the gain of the second gain stage and A3 is the gain of the output stage.

**IC 741 Bipolar operational amplifier:**

The IC 741 produced since 1966 by several manufactures is a widely used general purpose operational amplifier. Figure shows that equivalent circuit of the 741 op-amp, divided into various individual stages.

The op-amp circuit consists of three stages.

1. the input differential amplifier

2. The gain stage

3. the output stage.

A bias circuit is used to establish the bias current for whole of the circuit in the IC. The op-amp is supplied with positive and negative supply voltages of value ± 15V, and the supply voltages as low as ±5V can also be used.

**Bias Circuit:**

The reference bias current IREF for the 741 circuit is established by the bias circuit consisting of two diodes-connected transistors Q11 and Q12 and resistor R5. The widlar current source formed by Q11 , Q10 and R4 provide bias current for the differential amplifier stage at the collector of Q10. Transistors Q8 and Q9 form another current mirror providing bias current for the differential amplifier. The reference bias current IREF also provides mirrored and proportional current at the collector of the double –collector lateral PNP transistor Q13. The transistor Q13 and Q12 thus form a two-output current mirror with Q13A providing bias current for output stage and Q13B providing bias current for Q17. The transistor Q18 and Q19 provide dc bias for the output stage. Formed by Q14 and Q20 and they establish two VBE drops of potential difference between the bases of Q14 and Q18 .

**Input stage:**

The input differential amplifier stage consists of transistors Q1 through Q7 with biasing provided by Q8 through Q12. The transistor Q1 and Q2 form emitter – followers contributing to high differential input resistance, and whose output currents are inputs to the common base amplifier using Q3 and Q4 which offers a large voltage gain. The transistors Q5, Q6 and Q7 along with resistors R1, R2 and R3 from the active load for input stage. The single-ended output is available at the collector of Q6. the two null terminals in the input stage facilitate the null adjustment. The lateral PNP transistors Q3 and Q4 provide additional protection against voltage breakdown conditions. The emitter-base junction Q3 and Q4 have higher emitter-base breakdown voltages of about 50V. Therefore, placing PNP transistors in series with NPN transistors provide protection against accidental shorting of supply to the input terminals.

**Gain Stage:**

The Second or the gain stage consists of transistors Q16 and Q17, with Q16 acting as an emitter – follower for achieving high input resistance. The transistor Q17 operates in common emitter configuration with its collector voltage applied as input to the output stage. Level shifting is done for this signal at this stage. Internal compensation through Miller compensation technique is achieved using the feedback capacitor C1 connected between the output and input terminals of the gain stage.

**Output stage:**

The output stage is a class AB circuit consisting of complementary emitter follower transistor pair Q14 and Q20 . Hence, they provide an effective loss output resistance and current gain. The output of the gain stage is connected at the base of Q22 , which is connected as an emitter – follower providing a very high input resistance, and it offers no appreciable loading effect on the gain stage. It is biased by transistor Q13A which also drives Q18 and Q19, that are used for establishing a quiescent bias current in the output transistors Q14 and Q20.

**Ideal op-amp characteristics:**

1. Infinite voltage gain A.

2. Infinite input resistance Ri, so that almost any signal source can drive it and there is no

loading of the proceeding stage.

3. Zero output resistance Ro, so that the output can drive an infinite number of other devices.

4. Zero output voltage, when input voltage is zero.

5. Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified with out

attenuation.

6. Infinite common mode rejection ratio, so that the output common mode noise voltage is

zero.

7. Infinite slew rate, so that output voltage changes occur simultaneously with input voltage

changes.

**AC Characteristics:**

For small signal sinusoidal (AC) application one has to know the ac characteristics

such as frequency response and slew-rate.

**Frequency Response:**

The variation in operating frequency will cause variations in gain magnitude and its

phase angle. The manner in which the gain of the op-amp responds to different frequencies is

called the frequency response. Op-amp should have an infinite bandwidth Bw =∞ (i.e) if its open loop gain in 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency. The op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain after a certain frequency reached. There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C. Below fig is a modified variation of the low frequency model with capacitor C at the o/p.



There is one pole due to R0 C and one -20dB/decade. The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig. f1 is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase angle of the open loop volt gain are fu of frequency can be written as, The magnitude and phase angle characteristics from eqn (29) and (30)

1. For frequency f<< f1 the magnitude of the gain is 20 log AOL in dB.

2. At frequency f = f1 the gain in 3 dB down from the dc value of AOL in dB. This frequency f1 is called corner frequency.

3. For f>> f1 the fain roll-off at the rate off -20dB/decade or -6dB/decade.





From the phase characteristics that the phase angle is zero at frequency f =0.

At the corner frequency f1 the phase angle is -450 (lagging and a infinite frequency the phase angle is -900 . It shows that a maximum of 900 phase change can occur in an op-amp with a single capacitor C. Zero frequency is taken as te decade below the corner frequency and infinite frequency is one decade above the corner frequency.

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**Circuit Stability:**

A circuit or a group of circuit connected together as a system is said to be stable, if its

o/p reaches a fixed value in a finite time. (or) A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact the o/p of an unstable sys keeps on increasing until the system break down. The unstable system are impractical and need be made stable. The criterian gn for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability , ex: Bode plots.

Bode plots are compared of magnitude Vs Frequency and phase angle Vs frequency. Any system whose stability is to be determined can represented by the block diagram.



The block between the output and input is referred to as forward block and the block between the output signal and f/b signal is referred to as feedback block. The content of each block is referred ―Transfer frequency‘ From fig we represented it by AOL (f) which is given by AOL (f) = V0 /Vin if Vf = 0. -----(1)

where AOL (f) = open loop volt gain. The closed loop gain Af is given by

AF = V0 /Vin

AF = AOL / (1+(AOL ) (B) ----(2)

B = gain of feedback circuit.

B is a constant if the feedback circuit uses only resistive components. Once the magnitude Vs

frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

**1. Method:1:**

Determine the phase angle when the magnitude of (AOL ) (B) is 0dB (or) 1. If phase angle is > .- 1800 , the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

**2. Method 2:**

Determine the phase angle when the magnitude of (AOL ) (B) is 0dB (or) 1. If phase angle is > .- 1800 , If the magnitude is –ve decibels then the system is stable. However, the some systems the phase angle of a system may reach -1800 , under such conditions method 1 must be used to determine the system stability.

**Slew Rate:**

Another important frequency related parameter of an op-amp is the slew rate. (Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/μs).

**Reason for Slew rate:**

There is usually a capacitor within 0, outside an op-amp oscillation. It is this capacitor which prevents the o/p voltage from fast changing input. The rate at which the volt across the capacitor increases is given by dVc/dt = I/C --------(1)

I -> Maximum amount furnished by the op-amp to capacitor C. Op-amp should have the either a higher current or small compensating capacitors.

For 741 IC, the maximum internal capacitor charging current is limited to about 15μA. So the slew rate of 741 IC is SR = dVc/dt |max = Imax/C .

For a sine wave input, the effect of slew rate can be calculated as consider volt follower -> The input is large amp, high frequency sine wave .

If Vs = Vm Sinwt then output V0 = Vm sinwt . The rate of change of output is given by dV0/dt = Vm w coswt.





The max rate of change of output across when coswt =1

(i.e) SR = dV0/dt |max = wVm.

SR = 2ΠfVm V/s = 2ΠfVm v/ms.

Thus the maximum frequency fmax at which we can obtain an undistorted output volt of peak value Vm is given by

fmax (Hz) = Slew rate/6.28 \* Vm . called the full power response. It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

**DC Characteristics of op-amp:**

Current is taken from the source into the op-amp inputs respond differently to current and Voltage due to mismatch in transistor.

DC output voltages are,

1. Input bias current

2. Input offset current

3. Input offset voltage

4. Thermal drift

**Input bias current:**

The op-amp‘s input is differential amplifier, which may be made of BJT or FET.

In an ideal op-amp, we assumed that no current is drawn from the input terminals.

The base currents entering into the inverting and non-inverting terminals (IB - & IB respectively).

Even though both the transistors are identical, IB

- and IB + are not exactly equal due to internal imbalance between the two inputs.

Manufacturers specify the input bias current IB



If input voltage Vi = 0V. The output Voltage Vo should also be (Vo = 0)

IB = 500nA We find that the output voltage is offset by,

*Vo* *I B*@b c *Rf* Q 2` a

Op-amp with a 1M feedback resistor

Vo = 5000nA X 1M = 500mV

The output is driven to 500mV with zero input, because of the bias currents.

In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated. Where a compensation resistor Rcomp has been added between the non-inverting input terminal and ground as shown in the figure below.



Current IB flowing through the compensating resistor Rcomp, then by KVL we get,

-V1+0+V2-Vo = 0 (or)

Vo = V2 – V1 ——>(3)

By selecting proper value of Rcomp, V2 can be cancelled with V1 and the Vo = 0. The value of Rcomp

is derived a

V1 = IB+Rcomp (or) IB+ = V1/Rcomp ——>(4)

The node‗a‘ is at voltage (-V1).Because the voltage at

the non-inverting input terminal is(-V1).

So with Vi = 0 we get,

I1 = V1/R1 ——>(5)

I2 = V2/Rf ——>(6)

For compensation, Vo should equal to zero (Vo = 0, Vi = 0). i.e. from equation (3) V2 = V1. So that,

I2 = V1/Rf ——>(7)

KCL at node ‗a‘ gives,

IB- = I2 + I1

Rcomp = R1 || Rf ———>(9)

i.e. to compensate for bias current, the compensating resistor, Rcomp should be equal to the parallel combination of resistor R1 and Rf.

**Input offset current:**

 Bias current compensation will work if both bias currents IB

+ and IB- are equal.

 Since the input transistor cannot be made identical. There will always be some small

difference between IB

+ and IB-. This difference is called the offset current

|Ios| = IB+-IB- ——>(10)